Implementation of a Genetic Algorithm on a Virtex-II Pro FPGA

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ABSTRACT

This paper presents the implementation of a Genetic Algorithm on a XUPV2P platform with a Virtex-II Pro FPGA. A Genetic Algorithm (GA) is a search technique finding exact or approximate solutions to optimization and search problems. It is a computer simulation approach in which a population of abstract representations of candidate solutions to an optimization problem evolves toward better solutions. The aim is the optimization of a given function, called fitness function, which is evaluated upon the initial population as well as upon the solutions after successive generations. The motivation for implementing GAs in hardware stems from the fact that they are very CPU intensive while they are also intrinsically parallel algorithms and the basic operations of a GA can execute in a pipelining fashion. Our architecture incorporates a Power PC, and built-in hardcore resources like multiplier blocks and BRAMs in order to create an efficient hardware-based genetic algorithm. We have fine tuned the architecture so as to be more parallel, and added complex fitness functions. The design executes on 100 MHz and although complex in logic, it has low silicon requirements as it utilizes 16% slices, 7% BRAMs and 11% multiplier blocks, plus the Power PC. The result is a functional prototype on which experiments for a range of different genetic parameters can be conducted. We explore the GA's behavior with real-world experiments for different fitness functions and different number of generations. Our design is the first single-chip fully embedded approach that optimizes six fitness functions, which is more than any other proposed solution, while its current implementation supports populations of up to 32 members. The experiments show that our system outperforms in terms of execution time the existing and proposed hardware systems from 23% up to 5895%.

Categories and Subject Descriptors

B.7.1 [**Hardware**]: Integrated Circuits—*Algorithms implemented in hardware*; D.2.8 [**Software Engineering**]: Metrics—*complexity measures, performance measures*

General Terms

Algorithms, Design, Performance