

A Reconfigurable PID Controller

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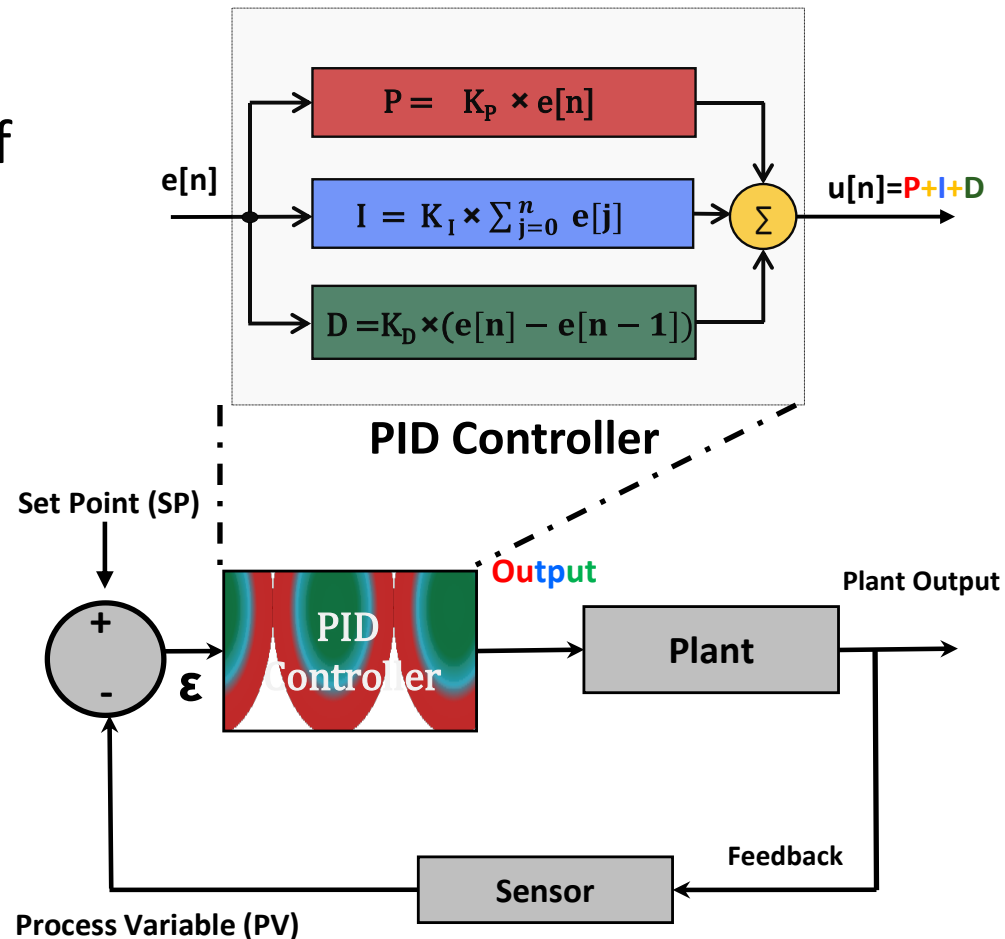
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FPGAs in industrial control

- Short response time and low-latency
 - the shorter the loop time, the faster the motor's respond to changes
- Reconfiguration for reliability
 - configuration scrubbing
- Complex control systems
 - several PID control loops are needed
 - sequential execution of each PID loop implemented in SW
 - > problem: increased time delay between input/output

Generic PID controller

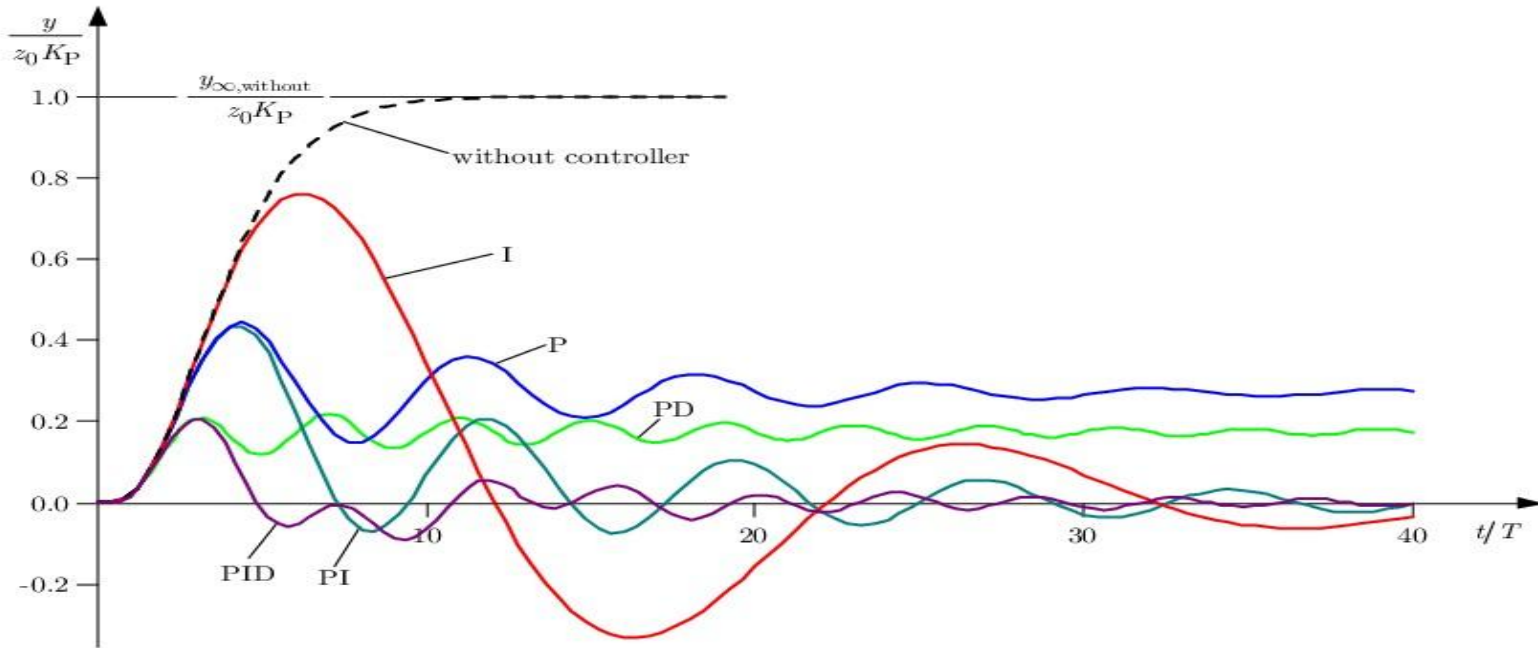
- P-I-D terms
 - **Proportional**: function of instantaneous error
 - **Integral**: function of accumulated errors
 - **Derivative**: rate of change of error
- Job of PID
 - $PV = SP$ ($\epsilon = 0$)
- PID variants
 - P-only, I-only, PI, PD etc



Best PID variant/Best solution?

- Depends on the requirements
 - most common type is PI
- Best solution is adaptive (non-linear) controllers
 - linear controllers have sufficient accuracy for small operating range only
- Multiple controllers available?
 - P-only, I-only, PI, PD, PID, PI-PD, PIDA etc, and switching amongst them: **operating regime**
- Other controllers better than PID?
 - FOC, Fuzzy, NN, Linear-Quadratic-Gaussian (LQG)
 - still, PID dominates the market

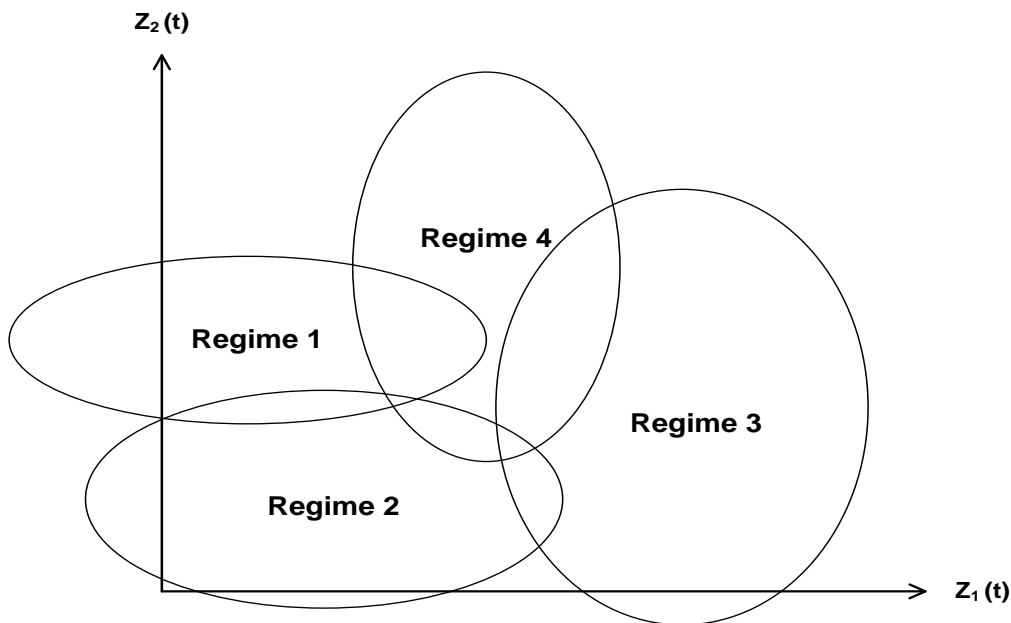
Behavior of PID variants



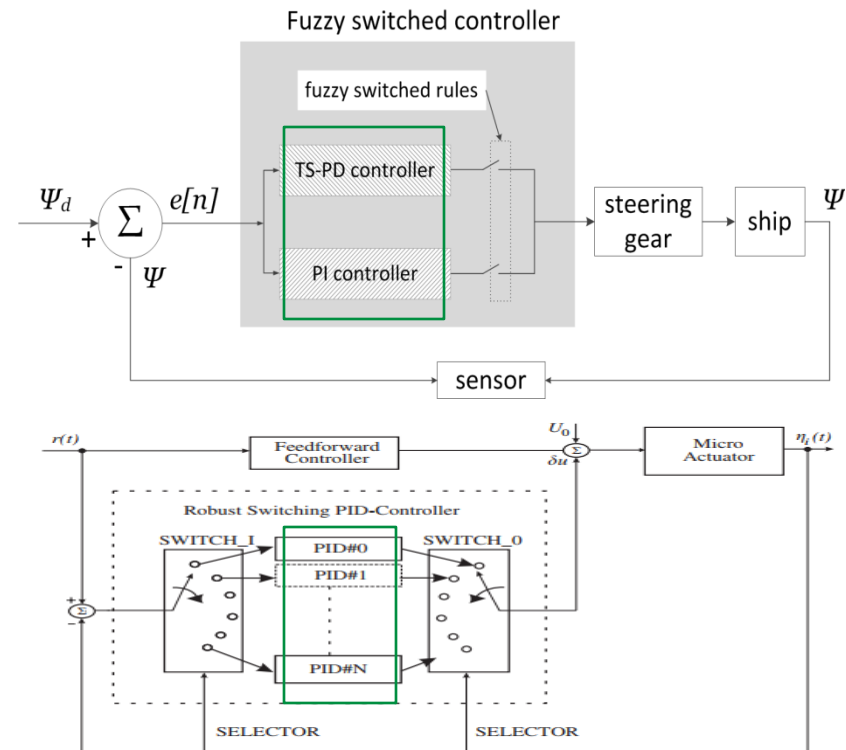
Parameter/Controller ↓	<i>P</i> -only	<i>PI</i>	<i>PD</i>	<i>PID</i>
Rise Time	Decrease	Minor Decrease	No Effect	Minor Decrease
Overshoot	Increase	Increase	Decrease	Minor Decrease
Settling Time	Small change	Increase	Decrease	Minor Decrease
Steady State error	Decrease	Eliminate	No Effect	Minor Decrease
Stability	Degrade	Degrade	Good	Good for K_D small

Adaptive controllers

- 2 ways: **Switching controllers**, and **Tuning gains in existing controller**
- **Switching controllers** is based on the concept of **operating regime**
 - decompose the operating envelope of a control process into regimes
 - an array of PID controllers designed separately for each regime gives better performance than a single controller



The vector $\mathbf{Z}(t)=(Z_1(t),Z_2(t))$ covers the entire operating range of the process.



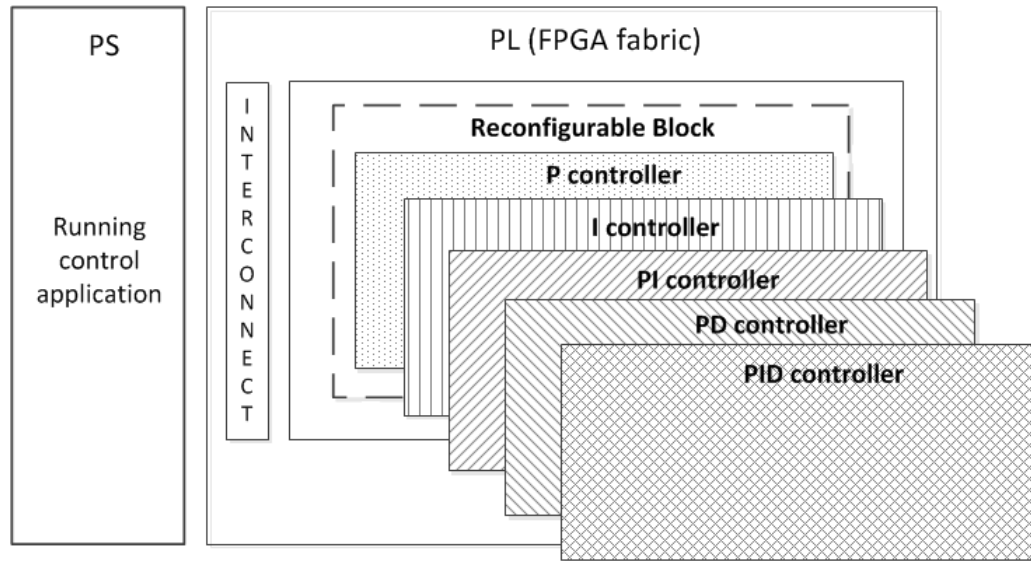
Static/Reconfigurable parts in proposed PID controllers

reference	Static	Reconfigurable
[11-13]	<ul style="list-style-type: none">- controller type- type of operations- # operations	<ul style="list-style-type: none">- gain parameters (K_p, K_i, K_d)
[14]	<ul style="list-style-type: none">- controller type- type of operations- # operations- gain parameters (K_p, K_i, K_d)	<ul style="list-style-type: none">- switching of the gain parameters
our work	<ul style="list-style-type: none">- gain parameters (K_p, K_i, K_d)	<ul style="list-style-type: none">- controller type- type of operations- # operations

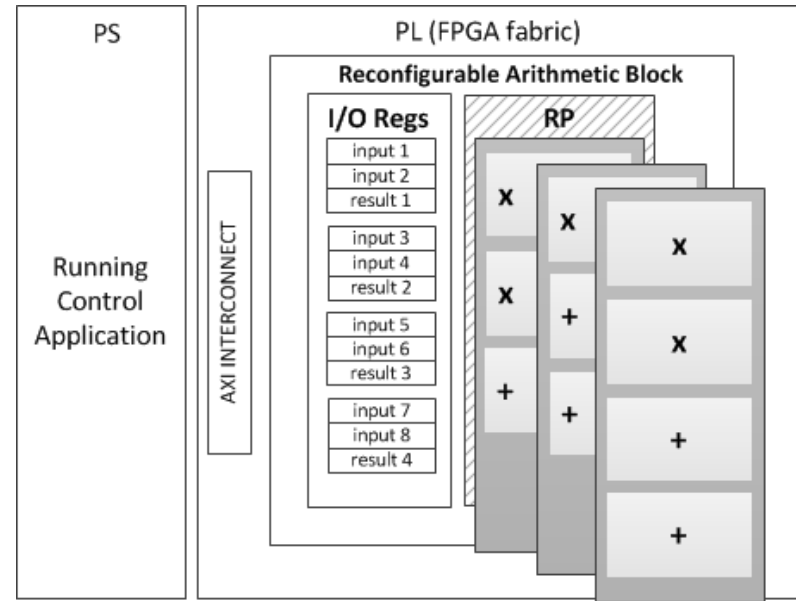
- few works have studied reconfiguration [11-14]
- in our work gain parameters are changed by writing values in registers

Our work

Concept

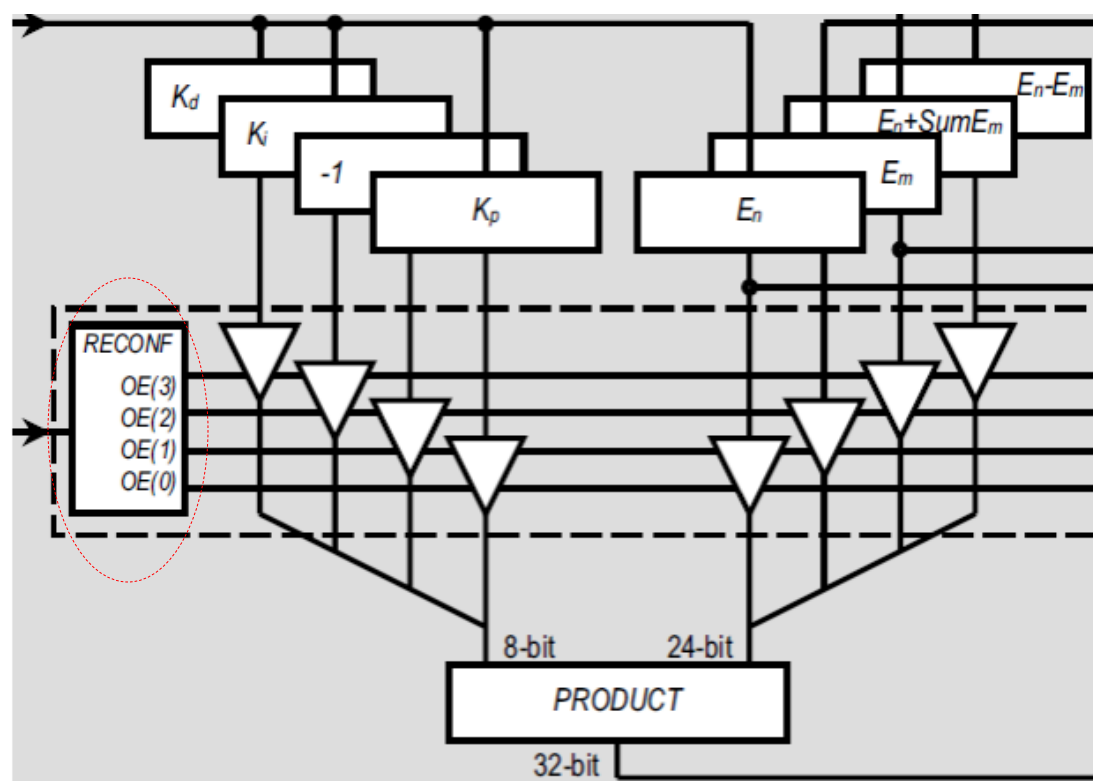


Implementation

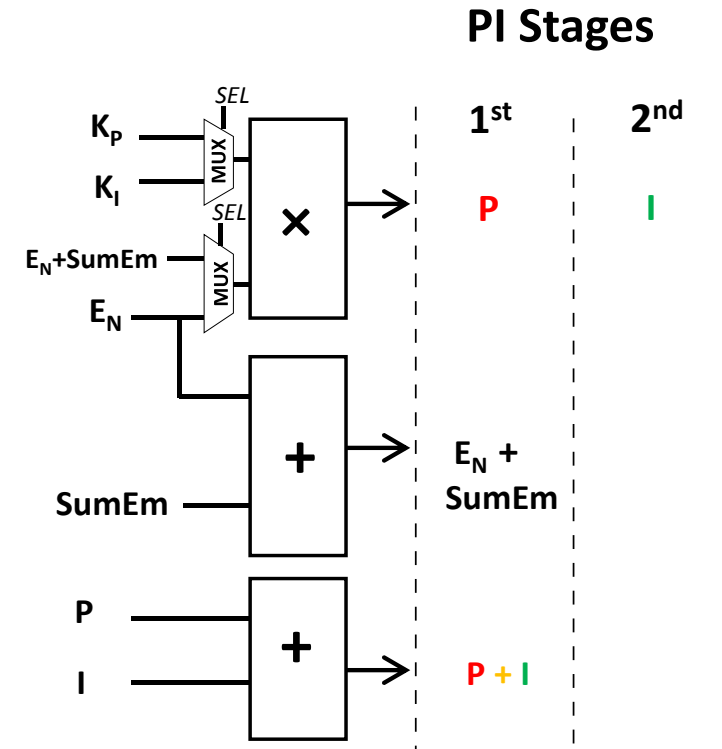


- One more application on partial reconfiguration; still looking for killer-app
- Lessons learned from building a reconfigurable PID controller
- 1 partial bitstream per controller

Eliminating reconfigurations within the PID cycle: design in [14] VS. our design



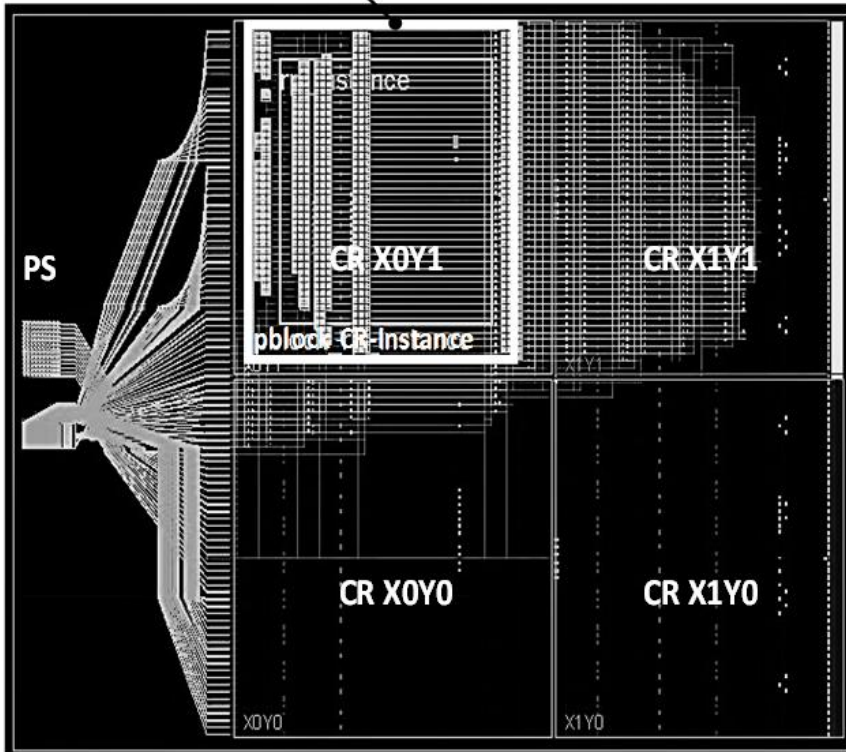
In [14], a circuit is reconfigured several times in every stage of the PID cycle, so as the proper gain parameter (K_p , K_i , K_d) is passed to the computational unit, depending on the stage of the PID cycle -> **frequent reconfiguration**



Gain parameters are passed via MUXes; "SEL" value depends on the stage of the PID cycle -> **no reconfiguration** (same for PD, PID, PI-PD etc.)

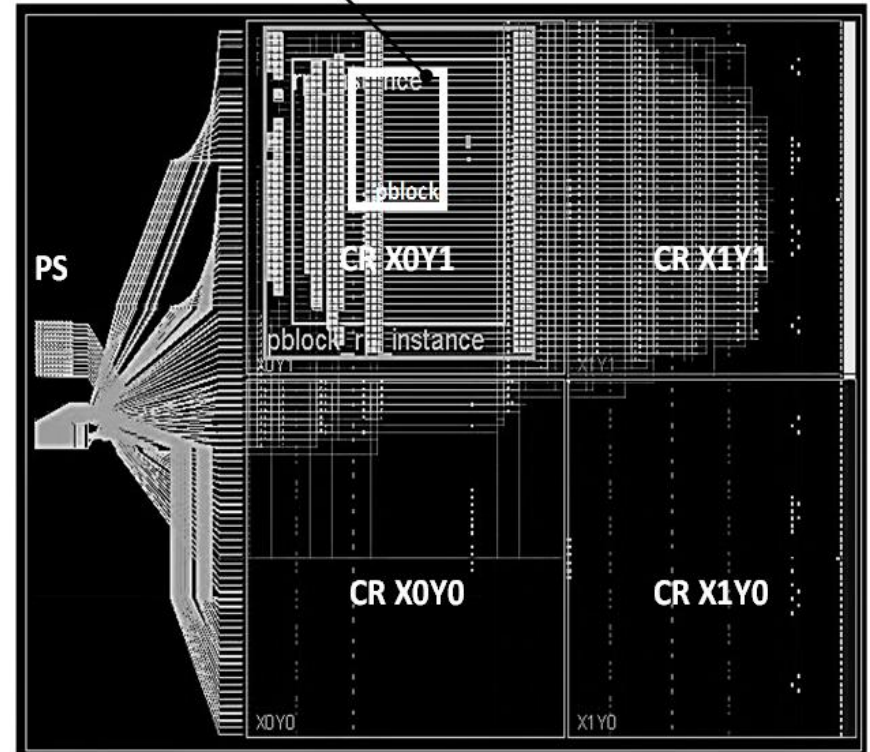
Resources and Reconfiguration in Zybo

The resources allocated in this Pblock can fit up to 15 arithmetic operations



- Partial bitstream size: **192,343 Bytes**
- Reconfiguration via PCAP

Minimum area needed to fit the operations of our reconfigurable PID controller



- Partial bitstream size: **55,727 Bytes**